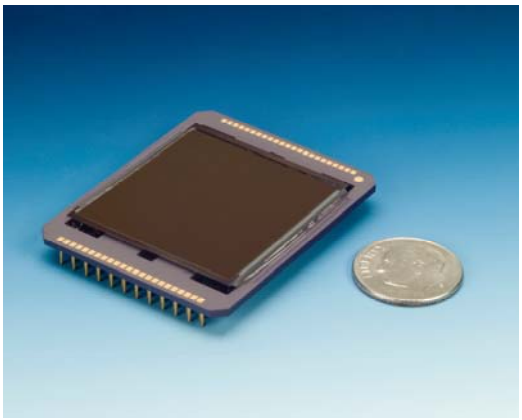
CCD 3041
Back-Illuminated 2K x 2K
Full Frame CCD Image Sensor

FEATURES



- **2048 x 2048 Full Frame CCD**
- **15 µm x 15 µm Pixel**
- **30.72 mm x 30.72 mm Image Area**
- **100% Fill Factor**
- **Back Illuminated**
- **Multi-Pinned Phase (MPP) Operation**
- **Readout Noise Less Than 3 e^- at 50kHz**
- **Four Low Noise Output Amplifiers**
- **Three Phase Buried Channel CCD**

GENERAL DESCRIPTION

The CCD 3041 is a 2048(H) x 2048(V) solid state Charge Coupled Device (CCD) full frame sensor. The CCD is intended for advanced scientific, aerospace, industrial, and medical imaging applications. The CCD 3041 active area is organized as an array of 2048 horizontal by 2048 vertical imaging elements. The pixel pitch is 15µm with a 100% fill factor. For dark reference, each readout line is preceded by 16 dark pixels. The imager is available in front- or back-illuminated configurations; however, this data sheet is for the back-illuminated configuration only. A split shift register design architecture has been adopted to accommodate high data rates by allowing the entire active pixel array to be read out simultaneously from all four output ports. In addition to 4 port readout, the standard package provides the ability to read out the image data from two output ports, located on the same side of the array. A simple modification allows the ability to read out the entire image frame from a single output port only, in order to simplify the drive electronics requirements.

A single-stage source follower output amplifier design has been selected for low noise performance. The readout noise floor is typically better than 3 e^- at a pixel rate of 50 kHz. Each output amplifier is capable of operating at up to 3 MHz with less than 20 e^- nominal read noise.

The CCD 3041 is mounted in a custom ceramic package for improved flatness uniformity and minimized mass. The PGA package is 36.8 x 45.7 mm with 46 pins.

FUNCTIONAL DESCRIPTION

The key functional elements are described next, and are shown in the block diagram.

Image Sensing Elements: The CCD photo-sensitive elements are made up of contiguous pixels with no voids or inactive areas. In addition to sensing light, these elements are used to shift image charge vertically. The full frame architecture requires that the device be mechanically shuttered during readout.

Backside Illumination: In a back-illuminated device, incident photons are collected on the backside of the CCD which has been thinned to about 18 microns. An accumulated surface potential helps direct the generated charge to the CCD depletion wells and is accomplished by performing a special surface treatment to the backside. The quantum efficiency of the CCD is further improved by applying antireflection coatings on the thinned CCD surface. This process can be tailored to optimize the device sensitivity over a range of spectral bands.

Vertical Charge Shifting: The architecture of the CCD 3041 provides video information as a sequential readout of 2048 lines, each containing 2048 photosensitive elements (in 1x1 mode, using a single output). At the end of the integration period, the ΦV_1, ΦV_2, and ΦV_3 gates are clocked to transfer charge vertically through the CCD array and to the horizontal readout register. Vertical columns are separated by channel stop regions to confine charge horizontally. The Vertical Transfer Gate (ΦVTG) is the final array gate before charge is transferred to the serial horizontal shift registers. For simplified operation ΦVTG may be tied to ΦV_3.

The imaging area is electrically divided into four quadrants. Each 1024 x 1024 segment may be clocked independently or combined as required. Horizontal serial registers along the top and bottom permit simultaneous readout of the upper and lower halves. The CCD 3041 also may be clocked such that the full array is read out of either the upper or the lower serial registers.

Horizontal Charge Shifting: ΦH_1, ΦH_2, and ΦH_3 are polysilicon gates used to transfer charge horizontally to the output amplifiers. The pixels in the horizontal registers are twice the size of the photosites to allow vertical charge binning, and a summing well is also provided to support horizontal charge binning. The array can be read out normally at 2K(H) x 2K(V) full resolution, as a 2K(H) x 1K(V), or 1K(H) x 1K(V). The horizontal shift registers are bi-directional so that the image frame may be read out through a single, or two amplifiers per serial register.

The transfer of charge into the horizontal registers follows the vertical charge transport sequence. These registers contain 16 additional register cells between the first pixel of each line and the output amplifier. (Note that the summing gate is part of the last prescan pixel.) The output of these pixels contains no signals and may be used as a dark level reference.

The last clocked gate in the horizontal registers, ΦSG, can be used to combine the signal charge of the pixels in the horizontal shift registers. This gate requires its own clock, which may be tied to ΦH_1 for normal full resolution readout. The output video is available following the high to low transition of ΦTG.

After the pixel has been sampled, the reset transistor, clocked appropriately with ΦR, resets the sense node potential to the level set by VRD.

Output Amplifier: The CCD 3041 has a low noise output amplifier at each end of the horizontal shift registers for a total of four output ports. The single-stage amplifier design has been optimized for low readout noise. Signal charge packets are serially clocked to a pre-charged capacitor, the sense node, whose potential changes linearly in response to the number of electrons delivered. This potential is applied to the input gate of an NMOS amplifier producing a signal at the output V_{out} pin. The capacitor is reset with ΦR to a pre-charge level prior to the arrival of the next charge packet (except when horizontal binning is performed). It is reset by use of the reset MOSFET. The output amplifier drain is tied to VDD. The source is connected to an external load resistor to ground. The voltage change at the source constitutes the video output from the device

Optional Frame Transfer Operation: The imaging area of the CCD 3041 consists of four contiguous sections that can be clocked independently such that the device will be capable of operating in frame transfer mode provided the outer sections are protected with opaque light shields, and the sensor is mounted in an optional package with the correct pinout. In frame transfer mode, the imaging section will be 2048(H) x (1024(V), and each storage section is 2048(H) x 544(V).

Die Orientation and Pin Designation: CCD orientation is indicated as shown in Figure 1 below, with pin 1 shown in the upper right (UR) quadrant when CCD is viewed from above. Pinouts are as shown in Figure 2. Note that the same pinouts are used for the front-illuminated version of the 3041 sensor but will require a modified timing diagram for operation.

Temperature Sensing: The package has two integrated thermistors (Murata, THERMISTOR 1K OHM, P/N NCP18XQ102J03RB) for temperature measurement.

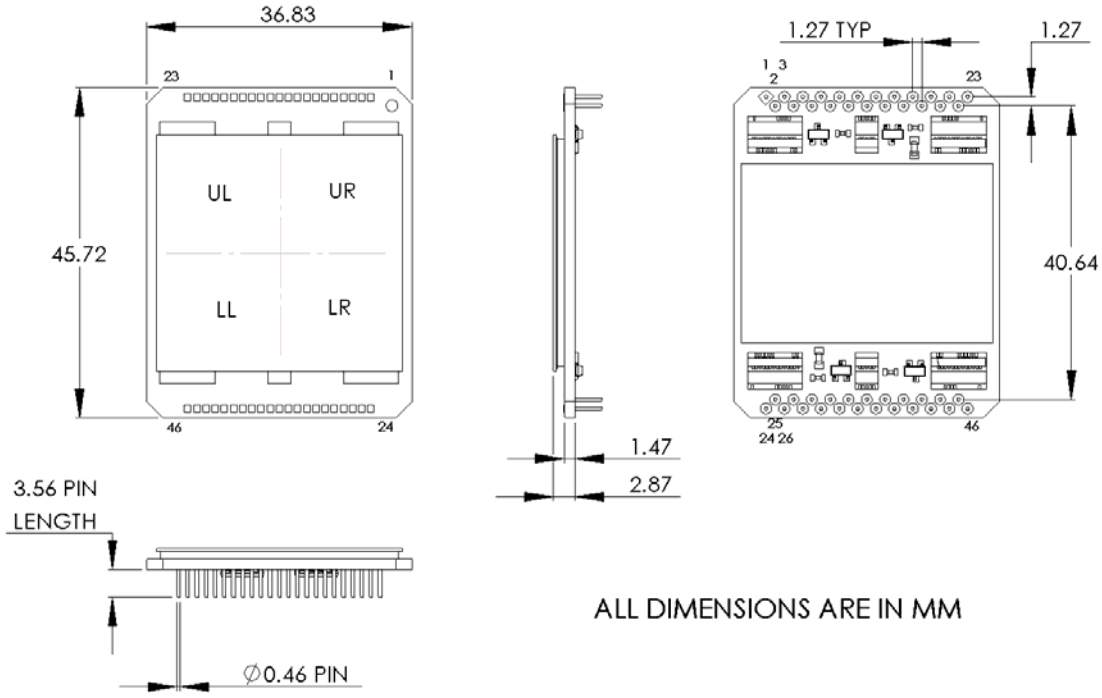
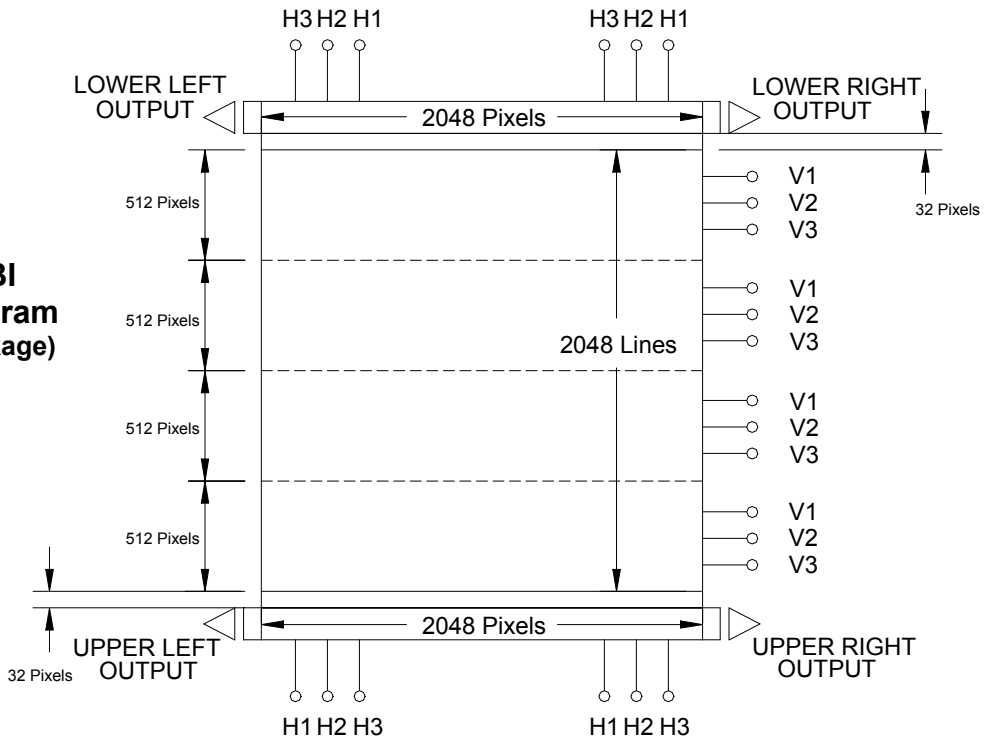


Figure 1: CCD 3041 BI Package

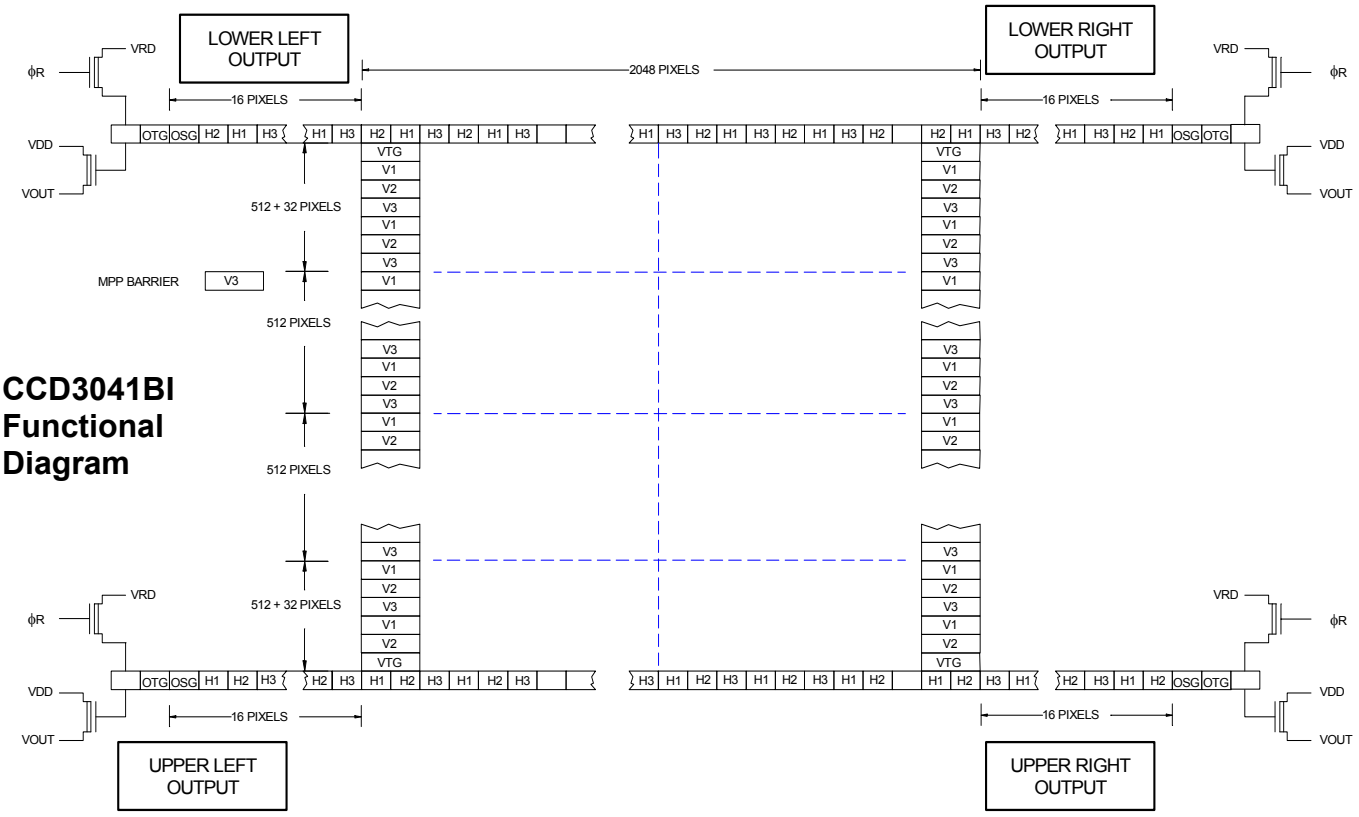
		PINOUT			
	1	VSS	THERM1-	24	
	2	V1	THERM1+	25	
	3	V2	V1	26	
	4	V3	V2	27	
	5	OR-UR	V3	28	
U	6	VRD-UR	VTG	29	L
P	7	VO-UR	OR-LR	30	O
P	8	VDD-UR	VRD-LR	31	W
E	9	HSG	VDD-LR	32	E
R	10	H3	VO-LR	33	R
	11	H1	VOG	34	
S	12	H2	H2	35	S
E	13	VOG	H1	36	E
C	14	VO-UL	H3	37	C
T	15	VDD-UL	HSG	38	T
I	16	VRD-UL	VDD-LL	39	I
O	17	OR-UL	VO-LL	40	O
N	18	VTG	VRD-LL	41	N
	19	V3	OR-LL	42	
	20	V2	V3	43	
	21	V1	V2	44	
	22	THERM2+	V1	45	
	23	THERM2-	VSS	46	

Figure 2: CCD 3041 BI Pinout

CCD 3041BI Block Diagram (in PGA package)



CCD3041BI Functional Diagram



Multi-Pinned Phase: MPP is a CCD technology which significantly reduces the dark current generation rate. CCDs are endowed with this capability by the addition of an ion implant step during the semiconductor manufacturing process.

This implant creates a built-in potential barrier in each pixel, which allows charge integration to be performed with all of the vertical clocks biased at their low levels (-8V). Under these conditions, the surface potential of the CCD is pinned at 0V, and the holes released by the neighboring p+ channel stops recombine with the electrons that are generated by surface defects which effectively neutralize the surface dark current.

While MPP operation significantly reduces the dark current of the CCD, a drawback of the MPP mode is reduced full well capacity. The potential barrier created by MPP implant does not hold as much charge as the normal buried channel operating mode which stores charge under one of the vertical gates biased high during integration. The CCD 3041 fabrication process has been optimized to maximize the charge capacity in MPP mode.

DEFINITION OF TERMS

Charge-Coupled Device: A charge-coupled device image sensor is capable of converting incident light photons into discrete packets of electron charge confined in individual pixels, then transfer the signal charge by sequential clocking of an array of gates to on-chip output amplifiers which produce the video output signals.

Vertical Transport Clocks ΦV_1, ΦV_2, and ΦV_3: The clock signals applied to the vertical transport registers to move signal charge from one pixel to the next.

Vertical Transfer Gate ΦVTG: The gate structure located adjacent to the last row of photosites and the horizontal transport registers. The charge packets accumulated in the photosites are shifted vertically across the array, then when they reach the last row of photosites, the signal charge is transferred to the serial register by appropriate clocking of the vertical transfer gate. Proper timing of the ΦVTG gate allows the vertical signal charges to be combined or binned.

Horizontal Transport Clocks ΦH_1, ΦH_2, ΦH_3: The clock signals applied to the horizontal transport registers to move signal charge from one pixel to the next.

Reset Clock ΦR: The clock applied to the reset transistor of the output amplifier.

Dynamic Range: The ratio of the pixel full well and the RMS noise floor in the dark. Dynamic range is typically expressed in dB.

Saturation Exposure: The minimum exposure level that produces an output signal corresponding to the maximum photosite charge capacity. Exposure is equal to the product of light intensity and integration time.

Responsivity: The output signal voltage per unit of exposure.

Spectral Response Range: The spectral band over which the response per unit of radiant power is more than 10% of the peak response.

Photo-Response Non-Uniformity: The difference of the response levels between the most and the least sensitive regions under uniform illumination (excluding blemished elements) expressed as a percentage of the average response.

Dark Signal: The output signal caused by thermally generated electrons. Dark signal is a linear function of integration time, and varies exponentially as a function of the chip temperature.

Pixel: Picture element or sensor element (also called photoelement or photosite).

DEVICE HANDLING PRECAUTIONS

Due to the negative bias conditions necessary for proper operation, the CCD 3041 is not equipped with built-in ESD protection circuitry. Strict ESD procedures and proper handling precautions must be performed to avoid accidental damage to the devices. The warranty does not apply to ESD damaged devices.

- Always store the devices with the shorting pins that are shipped with the devices securely attached to all of the pins.
- Never insert or remove the device from a live socket or operating camera. Turn off all electrical power first.
- Test stations must be specifically designed to minimize static charge build-up, including ionizing air blowers, and grounded floor mats.
- The relative humidity level in the working environment must be controlled between 40% - 60%.
- Never handle the devices without proper personal ESD protection items such as tested grounding straps, electrically conductive gloves or finger cots, ESD safe smocks, conductive shoe straps are also desirable.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range ..... -50 ºC to +75 ºC
Operating temperature range ..... -100 ºC to +40 ºC

GENERAL INFORMATION

PARAMETER		SPECIFICATION		UNIT
Active Pixels	Horizontal Vertical	2048 2048		Column Row
Pixel Size		15 x 15		μm^2
Active Image Area (H X V)		30.72 x 30.72		mm^2
Serial Prescan Pixels		16		
Parallel Prescan Pixels		32		
Number of Output Amplifiers		4		
Active Area Flatness		Typ: 20	Max: 30	µm

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
V_{DD}	DC Supply Voltage	18	24	28	V
V_{RD}	Reset Drain Voltage	13	14	18	V
V_{OG}	Output Gate Voltage	- 5	-2.5	1	V
V_{SS}	Substrate Ground	0	0	0	V

TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT
ΦH_1, ΦH_2, ΦH_3	Horizontal Register Clocks	+5	-5	V
ΦSG	Summing Gate Clock	+5	-5	V
ΦV_1, ΦV_2	Vertical Register Clock	+4	-9	V
ΦV_3	Vertical Register Clock	+4	-9	V
ΦR	Reset Clock	+10	0	V
ΦVTG	Array Transfer Gate Clock	+4	-9	V

AC CHARACTERISTICS

Standard test conditions are: 23 ºC, nominal MPP clocks, and DC operating voltages,

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
Z	Suggested Load Resistor	2	2.4	5	KΩ

PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	REMARKS
CTE	Charge Transfer Efficiency, Per Pixel Vertical Shift Registers Horizontal Shift Registers	 0.99995 0.99995	 0.999995 0.999995			
F read	Readout Frequency		1	3	MHz	
N read	Readout Noise		7	9	e-	Note 1
V_{SAT}	Saturation Output Voltage	170	300		mV	
FW (V)	Vertical Register Full Well Capacity	85	100		ke-	
FW (H)	Horizontal Register Full Well Capacity	650	750		ke-	
Nsat	Output Node Charge Capacity	700	800		ke-	
OCG	Output Amplifier Conversion Gain	3	4		µV/e-	
PRNU	Photo Response Non-Uniformity		10		% V_{SAT}	Measured at half saturation
I_{dark}	Dark Current (Mpp) (Rt)		200	352	e-/pix/sec	Note 2
DSNU	Dark Signal Non Uniformity (Rt)		80	160	e-/pix/sec	Note 3

Note 1: Measured at 1 MHz, -60°C
Note 2: Dark current doubles for every 7°C
Note 3: Standard deviation of 100-pixel thick horizontal line profile of dark image frame, excluding the outer 2 edge columns

CCD3041 OPERATING REQUIREMENTS

Package pinout and clock timing requirements: The front-illuminated and back-illuminated CCD3041 packaged sensors share the same pinout configuration but require different horizontal clock timing as shown in the next section. For proper charge transport, the H1 and H2 clocks are swapped between the front and back-illuminated devices.

Clock Timing Diagrams

BACK-ILLUMINATED CCD3041 SENSOR

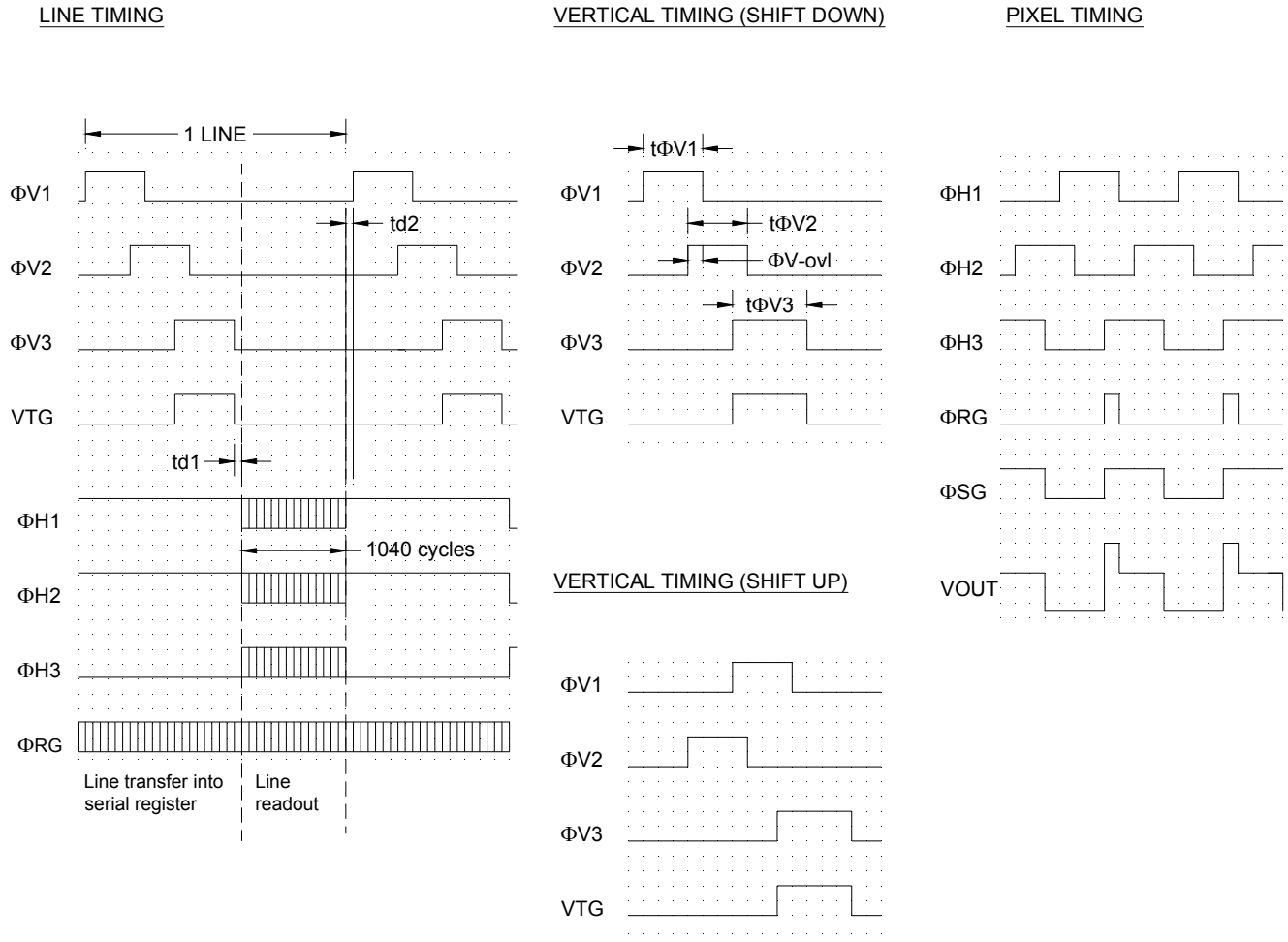


Figure 3. Back-illuminated CCD3041 Timing Diagrams

TYPICAL CLOCK TIMING

PARAMETER		SYMBOL	VALUE	UNIT	REMARKS
Horizontal clock frequency		f_H	400	kHz	
Horizontal clock pulse width		tΦH	1.25	µs	
Horizontal clock overlap		f_H-ovl	0.3	µs	
Horizontal blanking time		H-blank	600	µs	
Vertical clock frequency		f_V	2.5	kHz	
Vertical clock pulse width	V1, V2	tΦV1, tΦV2	200	µs	
	V3	tΦV3	300	µs	
Vertical clock rise and fall times		ΦVtr, ΦVtf	200	ns	
Vertical clock overlap		f_V-ovl	26	µs	
Reset clock pulse width		tΦR	300	ns	

Frame readout modes
The CCD3041 in packaged form is designed to accommodate 4-port readout or 2-port readout. In 4-port readout mode, the 4 quadrants of the active area are read out using the on-chip output amplifier of the corresponding quadrant. In 2-port readout mode, the vertical clocks must be modified to shift the data to the desired side (upper or lower) then the frame will be read out using the 2 on-chip output amplifiers of the selected half of the sensor. Single output port readout is not supported in the standard configuration.

Clock voltages
The same clock amplitudes can be used in the horizontal shift register and the output summing gate (± 5V) in unbinned mode. The devices are typically screen tested in this mode. Similarly, the phase-3 vertical gates can be clocked using the same clock amplitudes as the phase-1 and phase-2 gates in unbinned mode. However, for optimal full well charge handling capacity in binned pixel mode, we recommend that the summing gate high level be raised to +9V and the phase-3 vertical gates (including the vertical transfer gates), be offset by ~ +2V.

Power up and power down requirements
To prevent accidental damage to the on-chip output amplifiers during the power up sequence, the recommended bias voltage must always be applied first to all of the reset drain pins (VRD). Bias to Vdd can only be applied after the VRD pins have reached their voltage settings. During power down, power to VRD should be removed last.

Output JFET buffer and load resistor
A 20 kohm load resistor attached to the source of the output amplifier and a JFET buffer are mounted directly in the back-illuminated CCD3041 header as shown in Figure .

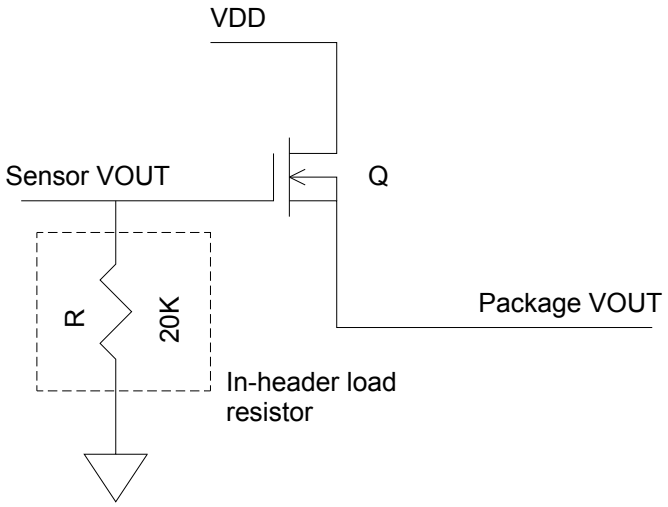


Figure 4. CCD output with load resistor and JFET buffer mounted in the header

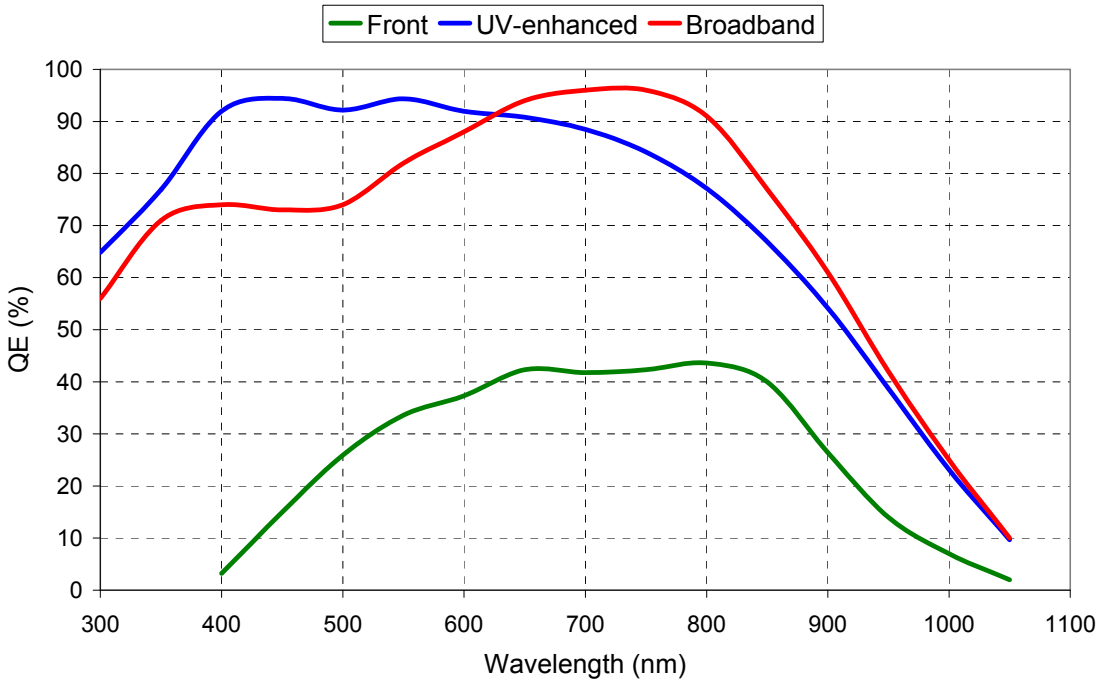


Figure 5. Typical 3041 QE curves

BLEMISH SPECIFICATIONS

The CCD 3041 is available in several different cosmetic grades as shown below. Grade 0 and custom graded devices are available. Please contact Fairchild Imaging with your requirements. Custom selected grades are also available. Consult your sales representative for custom grade requirements.

Grade	Point Defects	Column Defects	Clusters Defects	Cluster Size
1	50	3	5	10
2	100	6	10	25
3	500	20	40	50

Cosmetic Specifications Definition	
Point Defect	A black pixel or white pixel defect
Cluster Defect	A contiguous grouping of white or black pixel defects with a size less than or equal to Cluster Size
Column Defect	A contiguous grouping of 10 or more white or black pixel defects in a single column
Black Pixel	A pixel with an amplitude less than 50% of the local mean when measured at half the pixel full well
White Pixel	A pixel with more than 10X the local dark signal

WARRANTY

Within twelve months of delivery to the original customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging components, or camera products, if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that its products are fully inspected and tested at the factory prior to shipment, and that they conform to the stated specifications.

This product is designed, manufactured, and distributed utilizing the ISO 9000:2000 Business Management System.

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